PATENTS ACT 1977

IN THE MATTER OF
Application No. GB 9615001.6
in the name of NEC Corporation

DECISION

Introduction

1. This application was filed on 17 July 1996 in the name of NEC Corporation, and relates to a printed circuit board with a recess for mounting bare chips. It takes priority from Japanese application JP07202898 and was published on 19 February 1997 as GB 2303493.

Claim 1 of the application as originally filed read as follows:

> "A printed circuit board comprising a number of wiring circuit conductor layers and insulating layers alternately stacked on one or both surfaces of a substrate, and a recess within which a bare chip is mountable, wherein at least one outermost insulating layer comprises a photosensitive resin, and said recess is formed by photo etching said at least one outermost insulating layer ."

2. A search report under section 17 was issued on 25 October 1996 citing one document, US 4993148 (Adachi), as background. The first examination report under section 18(3) issued on 14 January 1999. In that report the examiner raised a novelty objection against claim 1 and four dependant claims on the basis of Adachi, apologising that the document had not been cited as a novelty citation (category X) on the earlier search report.

3. Amendments were filed, and a further examination report under section 18(3) issued on 20 July 1999. The examiner accepted that the amended claims overcame the novelty

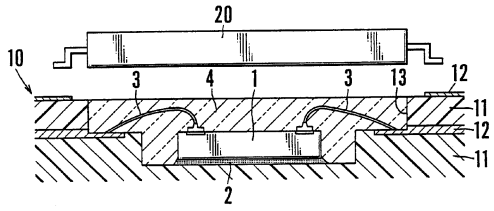
objection, but he considered that in the light of the disclosure in Adachi, the claims as amended lacked an inventive step.

4. After several more rounds of correspondence, further amended claims were filed, but still the examiner maintained the objection, based on Adachi, that the invention did not involve an inventive step. At one point, two further documents were cited by the examiner to show that one of the features that had been brought into the claims was common general knowledge in the art.

5. Further correspondence between the agent and the examiner failed to resolve the matter and consequently it came before me at a hearing on 2 February 2000. The applicant was represented by Mr Andrew Booth. Mr Moir (a colleague of Mr Booth's) and Mr Elbro (Patent Examiner) also attended

The application

6. The application is entitled "Printed Circuit Board" and relates to a method of forming a recess in an insulation layer of a multi-layer printed circuit board, so that an electronic component (referred to as 'a bare chip') can be mounted in the recess. The application explains that Chip-On-Board or COB technology is conventional, and figure 2 (reproduced right) shows part of a multi-layer board according to the prior art. The bare chip (**1**) is electrically connected to nearby bonding pads using very fine wires (**3**), and the chip is then encapsulated in resin (**4**) to protect the chip and the connecting wires.



Prior art

7. As the above figure shows, Chip-On-Board technology permits components to be packed more densely on a circuit board, since another component (**20**) can be mounted on the surface of the circuit board above the bare chip.

8. The application mentions a number of Japanese unexamined patent publications that propose similar arrangements for mounting bare chips on circuit boards, but goes on to point out towards the bottom of page 4:

> "In any of the conventional bare chip mounting techniques described in these patent publications, however, a recessed portion is formed in a printed circuit board by mechanical cutting using, e.g., a router."

9. In the prior art example shown above, a stepped recess is formed so that an inner conducting layer is exposed to provide the bonding pads for the wires (**3**). The electrical conductors that form part of the multi-layer circuit boards (**12** in the figure above) can be made of copper foil with a thickness of a few tens of microns. Forming the recess with a mechanical cutter therefore requires great accuracy. Small variations in the thickness of the stacked layers of the multi-layer circuit board, or the precision of the cutting tool can lead to very low yield, and result in high manufacturing costs.

10. The invention concerns a new method of forming the recess by using photosensitive resin for the uppermost insulating layer, or layers. The recess is then formed by photoetching the uppermost insulating layer or layers. According to the application, this means that:

> "... the formation of the recessed portion and the exposure of the internal wiring circuit conductor layer can be easily and reliably performed. This increases markedly the product accuracy of the printed circuit board, and so printed circuit boards can be manufactured with a high yield."

11. A paragraph on page 9 of the application describes the inventive concept as follows:

> "The characteristic feature of the bare chip mounting printed circuit board of the present invention is that a recessed portion, which is mechanically formed in a conventional bare chip mounting printed circuit board, is formed by photoetching. The rest of the printed circuit board of the present invention is identical with conventional printed circuit boards."

12. During the process of examination, the claims have been amended and there are now three independent claims, as follows:

1. A method of manufacturing a bare chip mounting multi-layer printed circuit board, comprising the steps of:

(a) forming a conductor layer on at least one of an upper surface and a lower surface of a substrate;

(b) photoetching said conductor layer to form a wiring circuit;

(c) entirely coating said conductor layer with an insulating layer containing a photosensitive resin; and

(d) photoetching said insulating layer to form a recessed portion therein for receiving a bare chip and exposing a portion of said wiring circuit for connection to the bare chip.

2. A method of manufacturing a bare chip mounting multi-layer printed circuit board, comprising the steps of:

(a) forming a first conductor layer on at least one of an upper surface and a lower surface of a substrate;

(b) photoetching said first conductor layer to form an inner wiring circuit;

(c) entirely coating said first conductor layer with an inner insulating layer;

(d) forming a through hole in said inner insulating layer;

(e) forming a second conductor layer on said inner insulating layer;

(f) photoetching said second conductor layer to form an outer wiring circuit;

(g) rendering said through hole conductive for electrically connecting said inner wiring circuit with said outer wiring circuit;

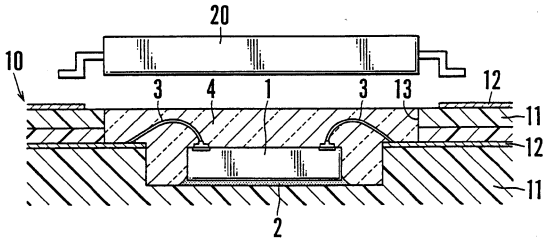
(h) coating the entire surface of said second conductor layer with an outer insulating layer containing a photosensitive resin; and

(i) photoetching said outer insulating layer to form a recessed portion therein for receiving a bare chip and exposing a portion of said outer wiring circuit for connection to the bare chip.

7. A bare chip mounting multi-layer printed circuit board having a number of insulating layers stacked from a surface layer of said printed circuit board and a number of wiring circuit conductor layers alternately stacked with said insulating layers, at least an uppermost two of said insulating layers comprising photosensitive resin, and a photoetched recessed portion formed in said insulating layers comprising

photosensitive resin, said recess having an opening for receiving a bare chip part and exposing a portion of one of said wiring circuits for connection to the bare chip, said recessed portion being a stepped recess comprising a first opening in an upper insulating layer of said insulating layers comprising photosensitive resin, and a second opening in a lower insulating layer of said insulating layers comprising photosensitive resin, said first opening being wider than said second opening.

13. These claims encompass a number of embodiments described in the specification, but in each case the inventive contribution is the means by which a recess is formed, and not the specific shape or construction of the resulting circuit board. Thus for example, the second embodiment of the invention shown in figure 6 of the application (see right) is very similar to the acknowledged prior art shown in figure 2 (above).



2nd Embodiment

The Law

14. The relevant part of section 1 reads:

"(1) A patent may be granted only for an invention in respect of which the following conditions are satisfied, that is to say —

(a) ....

(b) it involves an inventive step;

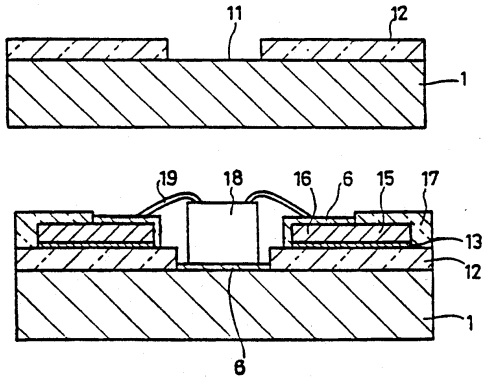
Section 3 reads:

"An invention shall be taken to involve an inventive step if it is not obvious to a person skilled in the art, having regard to any matter which forms part of the art by virtue only of section 2(2) above (and disregarding section 2(3) above)."

The Prior art

15. The prior art cited by the examiner in support of the inventive step objection is US 4993148 (Adachi et al), published on 19 February 1991. The abstract serves as a useful summary of the disclosure in Adachi (Note: LSI is an abbreviation of Large Scale Integration device):

> "A method is provided for forming a circuit board which comprises a copper plate and an insulating layer of photosensitive polymide resin formed on the copper plate, the insulating layer leaving an exposed portion of a surface of the copper plate where an LSI is to be mounted. After gold plating is applied to the exposed surface of the copper plate, the LSI is mounted fixedly. A connection pattern having bonding pads is formed by copper plating on the insulating layer. The bonding pads and the LSI are connected by gold wire bonding on the gold plating applied on the bonding pads."



16. Adachi discloses several embodiments of the invention, including a number of embodiments relating to multi-layer circuit boards. In its simplest form, as illustrated in figures 4A and 4E (reproduced right), a recess (**11**) is formed in an insulation layer (**12**) by means of photoetching. A thin layer of metal (eg gold, nickel or solder) is deposited in the bottom of the recess, and a bare chip or LSI device (**18**) is the mounted onto the metal substrate (**1**).

17. The purpose of the invention in Adachi is to improve heat dissipation from the electronic component (**18**) by providing a good thermal connection to a metal substrate. Adachi observes that conventional circuit boards constructed using organic high polymer materials such as paper phenol, glass epoxy or glass polyimide have insufficient thermal conductivity to cope with the heat levels generated by some components. As a result, the adhesive material of the insulating layer deteriorates and, in some cases, the layers of the circuit board can begin to peel because of the different rates of thermal expansion.

The issues

18. The question of whether or not an invention is obvious to a skilled person in the art must be decided on the technical facts of each particular case. Often it is a matter of considering a number of earlier published documents in order to decide whether an invention is obvious in the light of the combined teaching of the various pieces of prior art. In such a case, it must be likely that the skilled person would have considered the documents together.

19. On this occasion the situation is a little different. The invention concerns the use of photoetching to form a recess in the surface of a printed circuit board. Mr Booth submitted at the hearing that the closest prior art is that described in the application in suit, according to which a recess is formed by mechanical cutting (eg using a router). In the circumstances there can be no doubt that the inventors of the present application were familiar with the closest prior art. Moreover, the application describes the process of forming a recess by mechanical cutting as "conventional". I am therefore inclined to regard the prior art method disclosed in the application as common general knowledge.

20. Only one other document (Adachi) has been cited by the examiner as showing that the invention lacks an inventive step. The question that then arises is whether the notional skilled person, being aware of the conventional prior art methods disclosed in the present application, would have been led to the present invention by the additional disclosure of Adachi.

21. Mr Booth submitted that the notional skilled person would not be led to the invention from a consideration of Adachi because the problem being addressed in Adachi is completely different. Adachi is concerned with a method of mounting a chip on a printed circuit board so as to improve heat dissipation by providing a good thermal connection to a metal substrate. The problem facing the applicants in the present application was how to improve the accuracy of the process of forming a recess. According to Mr Booth, the notionally skilled person would quickly realise that Adachi was concerned with preventing problems caused by poor heat dissipation and would consequently reject it as being irrelevant to the current problem. Mr Booth argued that the notionally skilled person might easily dismiss Adachi before reaching the passage where photoetching is described as a means of forming the recess, but

that even if he/she read the entire document, it would not be obvious to take a small part of the disclosure and lift it completely out of its immediate context. Rather the reader would link the problem and the solution in his mind, and because the problem was not of immediate concern he would most likely disregard the solution because of its close association with the problem.

22. In connection with this latter point, Mr Booth referred me to Mr Justice Aldous' judgment in *Vax Appliances Limited v Hoover plc* [1991] FSR 307. Unfortunately Mr Booth did not indicate a specific part of Aldous J's judgment, and it is not clear to me that it is relevant to the matter before me. The most likely passage appears to be the following paragraph on page 310:

> "Commercial success is only of great weight to support the argument that an improvement could not have been obvious, otherwise it would have been made before. In the present case, the defendants contended that the invention was obvious over Reima and there is no evidence that anybody in this country ever read Reima. If so, the improvement may not have been made before because nobody read Reima or because it was not obvious. Further, so far as the Brycki patent is concerned, the invention was made soon after Brycki was marketed. Thus the argument cannot apply to the attack based on Brycki."

23. In this passage, Aldous J envisages a situation where nobody has read a particular patent specification. However, he does so not in the context of whether the disclosure should be taken fully into account as part of the prior art, but in response to the defendant's contention that there was no evidence that anybody had read Reima (a prior art document in *Vax Appliances v Hoover*). The defendant's argument being, as I understand it, that the invention would have been made earlier if somebody had read Reima. Aldous J deals with this by observing that "*the improvement may not have been made before because nobody read Reima or because it was not obvious*". In the circumstances I do not find this authority to be particularly relevant to the matter before me.

24. It is convenient at this point to deal with two other decided cases that Mr Booth drew to my attention. One is a decision of the EPO Board of Appeal in case T228/87. The other is *Olin Mathieson Chemical Corporation v Biorex Laboratories Ltd* [1970] RPC 157.

25. In decision T 228/87, the point that Mr Booth wanted to stress was that the disclosure of a single patent specification should not normally be regarded as common general knowledge. The Board of Appeal says at paragraph 4.1 that:

> "... while standard textbooks, encyclopaedias etc. will normally be accepted as evidence of common general knowledge, isolated pieces of patent literature, or scientific publications will - failing special circumstances so qualifying them - not generally be accepted to be such evidence."

26. I agree entirely with this statement of the Board of Appeal, and I do not believe that the teaching of Adachi falls within the category of common general knowledge. As I have stated above, I have concluded that the prior art described in the present application **is** common general knowledge but only because the application refers to it as "conventional".

27. In *Olin Mathieson Chemical Corporation v Biorex Laboratories Ltd*, the point that Mr Booth drew to my attention was the question whether a notional research group, knowing all the relevant prior art, would be led as a matter of course to try a particular variation. The relevant passage of Graham J's judgment is found at the bottom of page 187. Putting the question into the terms of this application: would the notional research group be led as a matter of course to try photoetching as a means of forming the recess in one or more insulating layers for the purpose of mounting a chip within the envelope of a printed circuit board? Mr Booth admitted that this case was not decided under the 1977 Act, but submitted that the approach remained appropriate nonetheless.

28. In this latter regard, the essence of Mr Booth's argument was that the reference to photoetching in Adachi is very insignificant; almost what I believe he described as a "throw away remark" or an aside. There was nothing, he suggested, to indicate to the reader that photoetching might also be a potential solution to an entirely different problem. I have some sympathy with this argument, although I am aware that it militates somewhat against an earlier submission of Mr Booth — that the suggestion of photoetching in Adachi would be disregarded by a reader because of its association with an entirely different problem. In the event it seems to me that photoetching is not directly part of the invention in Adachi. It is

simply one of a number of means by which a recess could be formed in the surface of a printed circuit board. At least one other method is suggested, screen printing. Moreover there appears to be no reason why the recess in Adachi could not be formed by mechanical cutting means as described in the present application.

29. However, while I accept that the reference to photolithography (or photoetching) is fairly insignificant when considered in the context of the disclosure of Adachi as a whole, I am conscious that the notionally skilled person would already be familiar with the art of photolithography. I know from personal experience that it has been used in the manufacture of printed circuit boards for many years, albeit for a different purpose — that is, to form the conductive tracks on the surface of the circuit board. I note that the examiner cited a further two patent specifications during the examination process to show that photoetching of conductive layers to form wiring circuits is well known in the art, and Mr Booth did not take issue with this during the hearing.

30. I have tried to put myself in the position of the notionally skilled person, and consider what I might have learned from a plain reading of Adachi. To begin with, and as Mr Booth argued, it is clear that Adachi is addressing a different problem. The process by which the printed circuit board is formed is also very different in Adachi; for example, the recess is formed at a much earlier stage in the manufacturing process. Nevertheless, there is a clear indication that an insulating layer may be comprised of photosensitive material, and photolithography used as a means of patterning (ie. forming recesses in) the insulating layer. I do not accept Mr Booth's argument that the skilled reader would dismiss the idea of photolithography as being an integral and inseparable part of the invention in Adachi. It is only one of two possible means disclosed in Adachi for forming the recess; the other being screen printing. It seems to me that the notionally skilled man would know that photolithography can be a very accurate and precise process. That is undoubtedly one reason why it has been used for so long as a means of forming very fine conductive tracks on printed circuit boards. In all the circumstances, and taking the best view I can of the matter, I have concluded that the skilled person would be led to consider photolithography as a more precise means of forming recesses in the insulating layers of a printed circuit board.

31. In reaching this conclusion I am aware that the teaching of Adachi could not be transferred directly into the conventional manufacturing process described in the present application. There would need to be some adaptation, but I am satisfied that the degree of adaptation would be very slight once the initial suggestion of using photolithography is provided. According to the present application, the characteristic feature of the invention is the use of photolithography to form the recess, and in my view this is an obvious alternative in the light of Adachi. Notwithstanding the statement in the application to the effect that the characteristic feature of the invention is the use of photolithography, there is no disclosure in the application that would suggest that there might be an inventive step in the specific adaption of photolithography to the applicant's existing manufacturing process.

32. I have considered whether there is disclosure in the application which could support a claim that would not contravene section 1(1)(b). However, there do not appear to be any saving amendments to the outstanding objection that the application lacks an inventive step. Accordingly, I therefore refuse the application GB 9615001.6

Appeal

33. This being a substantive matter, any appeal from this decision must be lodged within six weeks of the date of this decision.

Dated this 11th day of February 2000

Stephen Probert
Deputy Director, acting for the Comptroller
PATENT OFFICE